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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/091,432	03/07/2002	Shigetaka Asano	1076.1073	8832

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EXAMINER	
GHULAMALI, QUTBUDDIN	
ART UNIT	PAPER NUMBER
2637	

DATE MAILED: 06/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/091,432	ASANO, SHIGETAKA	
	Examiner	Art Unit	
	Qutub Ghulamali	2637	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 March 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☒ Claim(s) *15-23* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *9/17/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claims 3, 14, and 19 are objected to because of the following informalities:

Regarding claim 3, line 10, it is not clear what "the latency or more" means.

Regarding claims 14 and 15, lines 9 and 4, the abbreviation "GCA" must be spelled out to provide a clear meaning of the term used.

Regarding claim 15, line 15, after error, the word "and" must be deleted.

Regarding claim 19, line 2, the abbreviation "ADC" must be spelled out to provide a clear meaning of the term used.

Appropriate correction is required to informalities highlighted above.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

3. Claim 10 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 10 recites the limitation "the number of connected ones" in line 9. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-7, 14 are rejected under 35 U.S.C. 102(b) as being anticipated by Qureshi (USP 4,439,864).

Regarding claims 1 and 6, Qureshi discloses, an analog signal control method comprising:

converting the analog signal to a digital signal (ADC 62) (col. 2, lines 30-37);

performing an arithmetic processing (78) of the digital signal to generate a control signal for controlling the analog signal (col. 2, lines 23-60; col. 4, lines 8-20);

delaying the analog signal corresponding to a latency caused by the generation of the control signal to generate a delayed analog signal (in synchronism with the clock signal – crystal oscillator 96 generates clock signal which is provided to SPE and MPU 30) (col. 6, lines 15-42); and

controlling the delayed analog signal in accordance with the control signal (col. 3, lines 38-45).

Regarding claim 7, Qureshi discloses an analog signal controller comprises:

an ADC (figs. 2, 3, element 64) for analog-to-digital converting an analog signal to generate a digital signal (col. 2, lines 30-37);

a digital arithmetic circuit (78) connected to the ADC for performing an arithmetic processing of the digital signal to generate a control signal for controlling the analog signal (col. 2, lines 56-66);

a delay circuit for receiving the analog signal, and delaying the analog signal corresponding to a latency caused by the ADC and the digital arithmetic circuit to generate a delayed analog signal (col. 4, lines 8-20; col. 6, lines 15-20); and

an analog control circuit connected to the digital arithmetic circuit and the delay circuit for controlling the delayed analog input signal in accordance with the control signal (col. 2, lines 56-67; col. 7, lines 3-7).

Regarding claim 14, Qureshi discloses an automatic gain controller comprising:

a first control loop (62) for receiving an analog signal generate a control signal for setting a predetermined gain for use in amplifying the analog signal (col. 3, lines 39-46; col. 4, lines 8-60);

a delay circuit (204) receiving the analog signal, delaying the analog signal corresponding to a control delay(control delay=latency) caused by the first control loop generate a delayed analog signal (col. 4, lines 8-20); and

a GCA connected to the delay circuit and the first control loop for amplifying the delayed analog signal in accordance with a predetermined gain set by the control signal to generate an amplified analog signal (col. 3, lines 39-46; col. 4, lines 8-60).

As per claim 2, Qureshi discloses analog signal control method wherein:

the step of converting includes sampling the analog signal at a predetermined timing to generate a sampling value (abstract; col. 1, lines 21-35);

the step of generating a control signal includes generating the control signal in accordance with the sampling value (col. 1, lines 30-35; col. 2, lines 38-44); and

the step of delaying includes delaying the analog signal to control the analog signal in accordance with the control signal, the analog signal having a sampling value corresponding the predetermined sampling timing (the processor compares the average and the desired (predetermined) levels) (col. 6, lines 15-21).

Regarding claims 3, 4 and 5, Qureshi discloses an analog signal control method wherein:

the step of converting includes sampling the analog signal (A/D 62 provides inherent sampling) at a predetermined timing to generate a sampling value (abstract; col. 1, lines 21-35);

the step generating a control signal includes generating the control signal in accordance with the sampling value (col. 1, lines 30-35; col. 2, lines 15-44); and

the step of delaying includes delaying the analog signal by the latency to control the analog signal in accordance with the control signal, the analog signal having a sampling value produced by sampling the analog signal at a timing previous to the predetermined sampling timing (col. 6, lines 50-59).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Qureshi (USP 4,439,864) in view of Oishi et al (US Patent 6,563,859).

Regarding claim 8, Qureshi discloses an analog signal controller wherein: the analog signal controller operates in accordance with a clock signal (col. 1, lines 30-35; col. 2, lines 15-44). Qureshi however is silent regarding "the delay circuit includes a pair of switches which operate complementary to each other in synchronism with the clock signal, and delays the analog signal by switching the pair of switches". Oishi in a similar field of endeavor discloses a plurality of delay switches (fig. 12501-1 to 501-N), which operate complementary to each other in synchronism with the clock signal, and delays the analog signal by switching the plurality of switches (col. 11, lines 18-34). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use delay switches to delay analog signals (sampling period of the A/D converters) in synchronism with the clock signal as taught by Oishi in the circuit of Qureshi because it can provide equalization in frequency shift of the received signal to be extracted.

8. Claims 12 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Qureshi (USP 4,439,864) in view of Gurvich (US Patent 6,897,724).

Regarding claims 12 and 13, Qureshi discloses all of the claim limitations but is silent regarding a delay circuit includes a capacitor having a capacitance (variable) value for delaying the analog signal corresponding to a latency (error). Gurvich in a similar field of endeavor shows a system wherein capacitors are used in the delay circuit for delaying the signal, shows the capacitor could be a variable capacitor such as a varactor (variable capacitor) (col. 5, lines 25-50). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the

invention was made to use fixed or variable capacitors at the switch nodes as taught by Gurvich in the circuit of Qureshi because it can lend to proper group delay adjustments with the transmission of signal in the transmission line.

9. Claims 9-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Qureshi (US Patent 4,439,864) in view of Oishi (US Patent 6,563,859) as applied to claim 8 above, and further in view of Gurvich (US Patent 6,897,724).

Regarding claim 9 Qureshi in combination with Oishi discloses all of the claim limitations, except delay circuit includes a capacitor connected to a node between pair of switches and a ground. Gurvich in a similar field of endeavor discloses a system for adjusting group delay wherein delay circuit includes a capacitor (or a variable capacitor 501, 602) connected to a node (303) between pair of switches and a ground (figs. 3-6, elements 302, 403, 501) (col. 5, lines 26-37). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use fixed or variable capacitors at the switch nodes as taught by Gurvich in the circuit of Qureshi and Oishi because it can lend to proper group delay adjustments with the transmission of signal in the transmission line.

Regarding claim 10, Qureshi in combination with Oishi discloses all of the claim limitations, except the delay circuit further includes a selector circuit for selecting the plurality of delay stages in accordance with the sampling value of the analog signal. Gurvich in a similar field of endeavor discloses the delay circuit further includes a selector circuit for selecting the plurality of delay stages in accordance with the sampling value of the analog signal (col. 7, lines 50-67; col. 8, lines 1-2). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use selector circuit for selecting a plurality of delay stages as

taught by Gurvich in the circuit of Qureshi and Oishi because it can selectively mitigate delays with the transmission of signal in the transmission line.

Regarding claim 11, Qureshi in combination with Oishi discloses all of the claim limitations except a capacitor connected between a node and a ground. Gurvich in a similar field of endeavor further discloses a capacitor (302) connected between a node and a ground (fig. 3; col. 5, lines 26-30). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a capacitor at switch nodes as taught by Gurvich in the circuit of Qureshi and Oishi because it can achieve adequate group delay adjustments and suitable impedance matching of delay stages.

Allowable Subject Matter

10. Claims 15-18 and 19-23 would be allowable if rewritten or amended to overcome the claim objections, set forth in this Office action.

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

12.

US Patents:

Agrawal et al (USP 4,785,352) discloses a gain control apparatus in a feedback loop assures each signal is a close approximation on the input signal.

Terada et al (USP 4,884,192) shows an information processor capable of data transfer among plural digital data processors.

Burrowes et al (USP 4,785,352) discloses a sampled data amplitude detector as an AGC multiplier.

Dumas (USP 6,122,331) disclose a digital automatic gain control.

Mizoguchi (USP 5,305,351) shows an adaptive equalizer operation with a magnitude of fading.

Publications:

Turner P. G. et al "Chip Rate Processing For Software Defined Radios", 3G Mobile Communication Technologies, 2001. Second International Conference, March 2001, page(s): 292 - 296

Lovrich, A. Troullinos, G. Chirayil, R.: "An all digital automatic gain control", Texas Instrum. Inc., Houstc USA, Acoustics, Speech, and Signal Processing, 1988. ICASSP-88, 1988 International Conference on Publi Date: 11-14 April 1988, page(s): 1734 - 1737 vol. 3.

Camilleri, P.F. Sobelman, G.E., "Digital automatic gain control for hearing aids", Dept. Of Electrical Eng., Minnesota Univ., Minneapolis, MN, VLSI Signal Processing, VII, Oct. 1994, page(s): 3 - 12

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Qutub Ghulamali whose telephone number is (571) 272-3014. The examiner can normally be reached on Monday-Friday from 8:00AM - 5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jay Patel can be reached on (571) 272-2988. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

QG.
June 21, 2005.

JAY K. PATEL
SUPERVISORY PATENT EXAMINER